

Phase Shifter, 5-Bit Digital 6.0—18.0 GHz

M/A-COM Products Preliminary: Rev A

Features

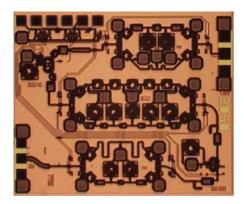
- ♦ 5 Bit Digital Phase Shifter
- ♦ 6.0 -18.0 GHz Operation
- ♦ 360° Coverage, LSB = 11.2°
- **♦ TTL Control Inputs**
- ♦ MSAG[®] Process
- ♦ RoHS Compliant

Description

The MAPCGM0004-DIE is a 5-bit Phase Shifter with Parallel TTL Input Control. This product is fully matched to 50 ohms on both the input and output. The part has 360° of phase coverage with LSB of 11.2°.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.



Primary Applications

- Satellite Communication
- Phased Array Radar
- Electronic Warfare

Electrical Characteristics: $T_B = 40^{\circ}C^1$, $Z_0 = 50\Omega$, $V_{EE} = -5V$

Parameter	Symbol	Typical	Units
Bandwidth	f	6.0 -18.0	GHz
Insertion Loss @ 12 GHz, Reference State	IL .	12	dB
Insertion Loss @ 18 GHz, Reference State	IL .	17	dB
Input VSWR, All States	VSWR	1.6:1	
Output VSWR, All States	VSWR	1.6:1	
RMS Phase Error	фкмѕ	10	0
RMS Phase Error, Calibrated	фкмѕ	6	o
Peak to Peak Gain Variation, All States	ΔG	< 2	dB
Current	lee	< 10	mA
Input Third Order Intercept	ITOI	30	dBm
Input 1-dB Compression Point	P1dB	19	dBm

1. T_B = MMIC Base Temperature

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Performance is based on engineering tests. Specifications are typical. Mechanical outline has been fixed.

Engineering samples and/or test data may be available. Commitment to produce in volume is not guaranteed.

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Maximum Ratings²

Parameter	Symbol	Absolute Maximum	Units
Input Power	P _{IN}	24	dBm
Source Supply Voltage	V_{EE}	-6.0	V
Junction Temperature	Tj	170	°C
Storage Temperature	T _{STG}	-55 to +150	°C

^{2.} Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions³

Characteristic	Symbol	Min	Тур	Max	Unit
Source Voltage	V _{EE}	-5.2	-5	-4.8	V
Control Voltage	V control pads				
Logic High		3	5	5	V
Logic Low		0	0	0.4	V

^{3.} Operation outside of these ranges may reduce product reliability.

Operating Instructions

This device is static and light sensitive. Digital circuit operation can be impaired under high intensity light, e.g. microscope light. Please handle with care. To operate the device, follow these steps.

- 1. Power Up: Apply $V_{EE} = -5 \text{ V}$.
- 2. Apply Logic Voltages to control Circuits as listed in Recommended Operating Conditions
- 3. Power Down: Set $V_{EE} = 0$



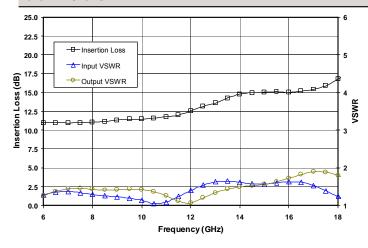
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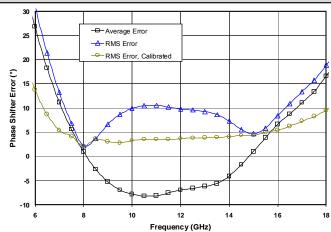
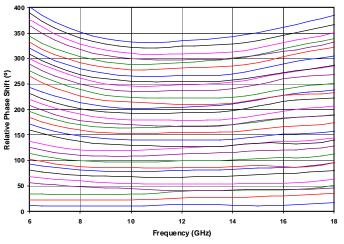


Figure 1. Reference State Insertion Loss, Input and Output VSWR vs. Frequency

Figure 2. Phase Shifter Figures of Merit: Average Error vs Reference State, RMS Error and Calibrated RMS Error over All States



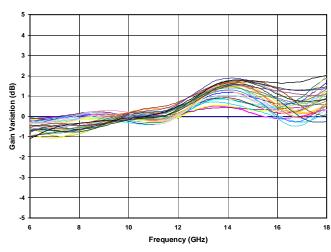
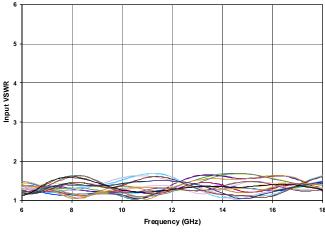


Figure 3. Relative Phase vs. Phase Shifter State

Figure 4. Relative Gain Change vs Phase Shifter State



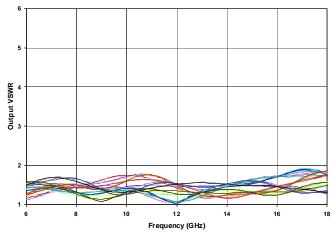


Figure 5. Input VSWR vs Phase Shifter State

Figure 6. Output VSWR vs Phase Shifter State

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Mechanical Information

Chip Size: 2.989 x 2.470 x 0.075 mm (117 x 97 x 3 mils)

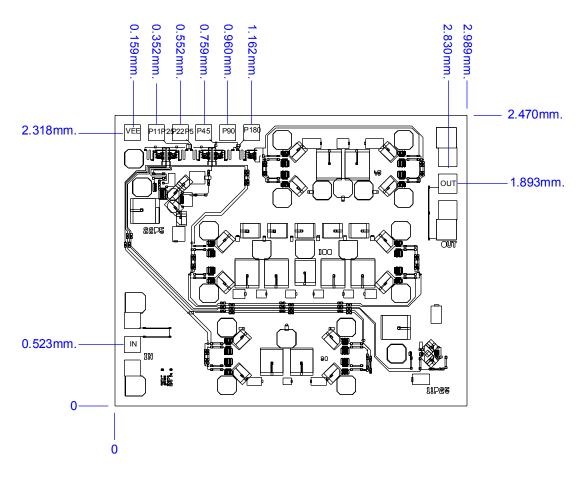


Figure 7. Die Layout

Bond Pad Dimensions

Pad	Size (μm)	Size (mils)
RF Out	150 x 150	6 × 6
RF In	125 x 125	5 x 5
Control Inputs	125 x 125	5 x 5
DC Supply Voltage V _{EE}	125 x 125	5 x 5

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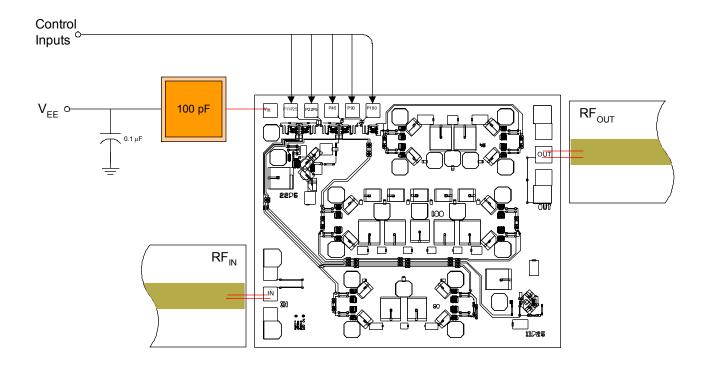


Figure 8. Recommended bonding diagram for pedestal mount. Support circuitry typical of MMIC characterization.

Die Handling:

Refer to Application Note AN3016.

Assembly Instructions:

Die Attach: Low thermal conductivity silver epoxies are acceptable for die attach of this MMIC. Follow the manufacturer's instructions. If solder is employed, use AuSn (80/20) 1-2 mil preform solder. Limit time @ 310°C to less than 5 minutes.

Wirebonding: Bond @ 160°C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.



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